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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,607	02/02/2000	Sarit Neter	YMEDIA.001A	6486

28112 7590 02/13/2004

GEORGE O. SAILE & ASSOCIATES
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER	
MOE, AUNG SOE	

ART UNIT	PAPER NUMBER
2612	22

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/496,607	NETER, SARIT	
	Examiner	Art Unit	
	Aung S. Moe	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/01/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,29,31,38 and 43-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,29,31,38 and 43-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 3, 38, 43-45, and 47-48 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments filed on December 01, 2003 have been fully considered but they are not persuasive.

Regarding claims 29, 31 and 46, the Applicant alleged that the amended limitations of claim 29, such that "wherein said interpolation comprises summing values of two or more said pixel sensor element", are not disclosed by the combination of Maenaka '023 and Lee '265.

In response, the Examiner respectfully disagrees because Maenaka '023 clearly shown in Figs. 2, 8 and 9 and further discussed in col. 6, lines 35+ that the interpolation process is performed by summing the values of two or more of the pixel sensor elements as claimed (i.e., noted the summing circuit 269-270 and the signals G22 as discussed in col. 6, lines 10+).

In view of the above, the amended features are clearly disclosed by Maenaka '023, thus, the Examiner will maintain the previous rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 38, 43, 44, 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (U.S. 4,768,085) in view of Lee at al. (U.S. 6,466,265) and Ochi et al. (U.S. 4,580,160).

Regarding claim 1, Hashimoto '085 discloses a color imaging system providing on-the-fly color interpolation using analog signals to reconstruct colors during sensor readout (Fig. 3, col. 3, lines 55-68), the imaging system comprising:

an array of pixel sensor elements wherein at least part of the array is arranged in rows and columns (Fig. 1; col. 3, lines 40+);

a color filter including a plurality of color filter components organized in a predefined pattern, the color filter overlaying at least a portion of the array (i.e., noted from Figs. 1 and 4 that the color filter components are organized in a predefined pattern);

a readout control circuit coupled to the array (i.e., noted the element 2a as shown in Fig. 2; col. 4, lines 5+);

an array controller coupled to the array (i.e., see Fig. 2; col. 4, lines 5+);

wherein the readout control circuit (2a) and the array controller (2a, 2a1 and 2a2) are configured to simultaneously read out values for a group of pixel elements from two different rows and two pixel elements from two different columns (i.e., Figs. 2, 7 and 12; col. 3, lines 54+, and col. 5, lines 60+) and

to reconstruct color components for at least a first pixel sensor element and a second pixel sensor element using color information (i.e., noted that the G signal is reconstructed from the pixels' signals such as G1 and G2 as shown in Figs. 2 and 3) from other pixels elements (i.e., noted the pixel elements nH/mH as shown in Fig. 1) within at least the first portion of the array while the readout control circuit is reading said first portion of the array (i.e., col. 4, lines 20+ and col. 5, lines 1+).

In addition, it is noted that although Hashimoto '085 shows the summing circuit (Fig. 2, the elements 2a3) to sum two or more (i.e., noted that at least two green signals are summed) of the analog values, Hashimoto '085 does not explicitly stated that the summing circuit (2a3) is a summing amplifier as amended in present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Ochi '160. In particular, Ochi '160 teaches that it is conventionally well known in the art at the time the invention was made to use a summing amplifier to sum two or more of the analog values in a color imager (i.e., see Fig. 4, the elements 45-47; col. 5, line 60 –col. 6, lines 15+) so that the distortion produced of the color output signals may be prevented, thereby improve the resolution of the color image signals (i.e., see col. 3, lines 35+).

In view of the above, having the system of Hashimoto '085 and then given the well-established teaching of Ochi '160, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Hashimoto '085 as taught by Ochi '160, since Ochi '160 states at col. 3, lines 35+ that such a modification would improve resolution of the color image signals by reducing the distortion of the color output signals.

Furthermore, it is noted that although Hashimoto '085 shows the use of a plurality of color amplifiers (i.e., noted from Fig. 3 that each of the amplifiers 3, 4 and 5 are corresponding to one the colors of light), Hashimoto '085 does not explicitly state that the amplifier has a programmable gain as recited in the present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Lee '265. In particular, Lee '265 teaches in order to achieve high pixels output rate for high frame rates, it is conventionally well-known in the art to use a plurality of color amplifiers (i.e., noted the amplifiers 92 and 93 as shown in Figs. 2e, 4 and 5) each corresponding to one of the colors (i.e., noted the R, G and B color signals read out from the pixels 1, 2, 3 and 4 as shown in Fig. 2b) of lights wherein each of the color amplifiers has a programmable gain (i.e., col. 4, lines 25+, col. 5, lines 25+; Figs. 4 and 5).

In view of the above, having the system of Hashimoto '085 and then given the well-established teaching of Lee '265, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Hashimoto '085 as taught by Lee

'265, since Lee '265 states at col. 1, lines 50+ that such a modification would achieve high pixels output rate for high frame rates thereof.

Regarding claim 3, Hashimoto '085 discloses wherein the readout control circuit is adapted to perform color interpolation using two pixel sensor elements read out in parallel (i.e., col. 3, lines 60+ and col. 6, lines 14+).

Regarding claim 43, it is noted that Hashimoto '085 does not explicitly states the use of CMOS Sensor, however, Lee '265 teaches that it is conventionally well-known in the art at the time the invention was made to use CMOS sensors in order to realize either high frame rate or high pixel count thereof (i.e., see col. 1, lines 25-55 of Lee '265). In view of this, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Hashimoto '085 as taught by Lee '265, since Lee '265 states at col. 1, lines 50+ that such a modification would achieve high pixels output rate for high frame rates thereof.

Regarding claim 44, although Hashimoto '085 shows the use of color filter components (i.e., col. 4, lines 5+ of Hashimoto '085), Hashimoto '085 does not explicitly state the use of a Bayer pattern color filter as recited in the present claimed invention.

However, Lee '265 teaches that it is conventionally well-known in the art at the time of the invention was made to use a Bayer pattern color filter as recited in the present claimed invention (i.e., col. 3, lines 20+ of Lee '265). In view of this, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of

Hashimoto '085 as taught by Lee '265, since Lee '265 states at col. 1, lines 50+ that such a modification would achieve high pixels output rate for high frame rates thereof.

Regarding claim 38, Hashimoto '085 discloses a color imager (i.e., Figs. 3, 5, 8 and 10) comprising:

a first light sensor which generates a first analog output signal related to the amount of a first color of light sensed (i.e., noted the sensor of the sensor 2 of the imager generates the first analog output signal such that the green signal G1 as shown in Fig. 8 and 9; see col. 6, lines 10+);

a second light sensor which generates a second analog output signal related the amount of said first color of light sensed (i.e., noted the sensor of the sensor 2 of the imager generates the first analog output signal such that the green signal G3 as shown in Fig. 8 and 9; see col. 6, lines 10+);

a third light sensor (i.e., The Blue sensor of the sensor 2) which generates a third analog output signal related to the amount of a second color of light sensed (i.e., noted the sensor of the sensor 2 of the imager generates the third analog output signal such that the blue signal B2 as shown in Fig. 8 and 9; see col. 6, lines 10+);

a fourth light sensor (i.e., The Red sensor of the sensor 2) which generates a fourth analog output signal related to the amount of a third color of light sensed (i.e., noted the sensor of the sensor 2 of the imager generates a fourth analog output signal such that the red signal R as shown in Fig. 8 and 9; see col. 6, lines 10+);

a circuit configured to read out the first, second, third, and fourth analog values at the same time (i.e., col. 3, lines 55-68 and col. 5, lines 60+); and

an interpolation circuit configured to receive said first output signal and said second output signal (i.e., col. 3, lines 55+), wherein said interpolation circuit provides an interpolation signals on the fly based on at least said first analog output signal and said second analog output signal (col. 6, lines 5+).

In addition, it is noted that although Hashimoto '085 shows the summing circuit (Fig. 2, the elements 2a3) to sum two or more (i.e., noted that at least two green signals are summed) of the analog values, Hashimoto '085 does not explicitly stated that the summing circuit (2a3) is a summing amplifier as amended in present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Ochi '160. In particular, Ochi '160 teaches that it is conventionally well known in the art at the time the invention was made to use a summing amplifier to sum two or more of the analog values in a color imager (i.e., see Fig. 4, the elements 45-47; col. 5, line 60 –col. 6, lines 15+) so that the distortion produced of the color output signals may be prevented, thereby improve the resolution of the color image signals (i.e., see col. 3, lines 35+).

In view of the above, having the system of Hashimoto '085 and then given the well-established teaching of Ochi '160, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Hashimoto '085 as taught by Ochi

'160, since Ochi '160 states at col. 3, lines 35+ that such a modification would improve resolution of the color image signals by reducing the distortion of the color output signals.

Furthermore, it is noted that although Hashimoto '085 shows the use of a plurality of color amplifiers (i.e., noted from Fig. 3 that each of the amplifiers 3, 4 and 5 are corresponding to one the colors of light), Hashimoto '085 does not explicitly state that the amplifier has a programmable gain as recited in the present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Lee '265. In particular, Lee '265 teaches in order to achieve high pixels output rate for high frame rates, it is conventionally well-known in the art to use a plurality of color amplifiers (i.e., noted the amplifiers 92 and 93 as shown in Figs. 2e, 4 and 5) each corresponding to one of the colors (i.e., noted the R, G and B color signals read out from the pixels 1, 2, 3 and 4 as shown in Fig. 2b) of lights wherein each of the color amplifiers has a programmable gain (i.e., col. 4, lines 25+, col. 5, lines 25+; Figs. 4 and 5).

In view of the above, having the system of Hashimoto '085 and then given the well-established teaching of Lee '265, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Hashimoto '085 as taught by Lee '265, since Lee '265 states at col. 1, lines 50+ that such a modification would achieve high pixels output rate for high frame rates thereof.

Regarding claim 47, please see the Examiner's comments with respect to claim 43 as discussed above.

Regarding claim 48, please see the Examiner's comments with respect to claim 44 as discussed above.

5. Claims 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto '085 in view of Lee '265 and Ochi '160 as applied to claims discussed above, and further in view of Wilder et al. (U.S. 5,262,871).

Regarding claim 45, although the combination of Hashimoto '085 and Lee '265 teaches the use of a control circuit is programmed to selectively reading groups of pixel elements to create a color reconstruction (i.e., noted Figs. 1 and 2 of Hashimoto '085; and Figs. 2a-3b of Lee '265), the combination of Hashimoto '085 and Lee '265 does not explicitly state that the readout control circuit is programmed to selectively skip some of the groups of pixel elements to create a lower resolution.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Wilder '871. In particular, Wilder '871 teaches that it is conventionally well-known in the art at the time of the invention was made to program the readout control circuit (i.e., noted the readout control circuit as shown in Fig. 1 of Wilder '871) for the purpose of selectively skip some of the groups of pixel elements to create a lower resolution image (i.e., i.e., noted that the groups of pixel elements as shown in Figs. 2 may be selectively skipped during the

specific resolution mode as discussed in col. 6, lines 50+; see col. 3, lines 20+ and col. 6, lines 2+ of Wilder '871).

In view of the above, having the combination of Hashimoto '085 and Lee '265 and then given the well-established teaching of Wilder '871, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Hashimoto '085 as taught by Wilder '871, since Wilder '871 states at col. 2, lines 50+ that such a modification would achieve high speed data capture rate for high frame rates thereof.

6. Claims 29, 31 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maenaka et al. (U.S. 5,555,023) in view of Lee at al. (U.S. 6,466,265).

Regarding claim 29, Maenaka '023 discloses a method of interpolating color components of an array of pixel sensor elements (col. 3, lines 40+ and col. 6, lines 45+), said method comprising:

reading a first rectangular portion of an array of pixel sensor elements simultaneously, wherein the first rectangular portion includes pixel sensor elements from at least two array columns and two array rows (i.e., Fig. 8; col. 1, lines 45-50, col. 2, lines 45+);

reading a second rectangular portion of the array of pixel sensor elements, wherein the second portion partly overlaps said first portion (i.e., Fig. 8; col. 1, lines 45+ and col. 2, lines 45+); and

reconstructing color components using interpolation for at least a third portion of the array while said third portion of the array is being read (i.e., Figs. 2 and 8-9; col. 2, lines 35+, col. 6, lines 35+ and col. 7, lines 20+), and wherein said interpolation comprises summing values of two or more said pixel sensor elements (i.e., see Fig. 2, the elements 269-270 and col. 6, lines 10-60).

Furthermore, it is noted that Maenaka '023 does not explicitly states the use of CMOS Sensors, however, Lee '265 teaches that it is conventionally well-known in the art at the time the invention was made to use CMOS Sensors in order to realize either high frame rate or high pixel count thereof (i.e., see col. 1, lines 25-55 of Lee '265). In view of this, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Maenaka '023 as taught by Lee '265, since Lee '265 states at col. 1, lines 50+ that such a modification would achieve high pixels output rate for high frame rates thereof.

Regarding claim 31, Maenaka '023 discloses wherein reconstructing color components (i.e., the R, G and B signal as shown in Fig. 8) using interpolation is performed in real-time (i.e., noted the color components are interpolated as read out from the CCD sensor in real-time as claimed).

Regarding claim 46, although Maenaka '023 shows the use of color filter components (i.e., Fig. 8 of Maenaka '023), Maenaka '023 does not explicitly state the use of a Bayer pattern color filter as recited in the present claimed invention.

However, Lee '265 teaches that it is conventionally well-known in the art at the time of the invention was made to use a Bayer pattern color filter as recited in the present claimed invention (i.e., col. 3, lines 20+ of Lee '265). In view of this, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Maenaka '023 as taught by Lee '265, since Lee '265 states at col. 1, lines 50+ that such a modification would achieve high pixels output rate for high frame rates thereof.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Ohzu '070 shows a color imaging system having CMOS sensor for providing a color image signal by using a summing amplifier (Fig. 29, the elements 805) for summing the values of two or more of the pixel elements thereof.

2. Liang '233 shows a MOS sensor having a programmable gain amplifier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aung S. Moe whose telephone number is 703-306-3021. The examiner can normally be reached on Mon-Fri (9-5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 703-305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aung S. Moe
Primary Examiner
Art Unit 2612

A. Moe
February 6, 2004